

Appl. No. 09/774,549  
Arndt. Dated August 12, 2004  
Reply to Office action of May 17, 2004

## REMARKS/ARGUMENTS

### Claims define allowable subject matter over the applied art

Claims 1-45 were provisionally rejected under 35 USC 101 as claiming the same invention as that of claims 1-47 of co-pending application number 09/774,552. Claims 1-21, 25, 28, 32-37 and 40-45 were rejected under 35 U.S.C. 102 (e) as being anticipated by Polichar et al (US patent 6,205,199). Claims 22-24, 26-27, 29-31 and 38-39 were objected to as being dependent upon a rejected base claim. No new matter has been added.

Claims 1-45 remain pending in this application.

### Double Patenting

The rejection of claims 1-45 under 35 USC 101 as claiming the same invention as that of claims 1-47 of application No. 09/774,552 is respectfully traversed. Applicants' invention as claimed in independent claims 1 and 44 discloses an image data acquisition system comprising a host computer having at least one host processor executing operations with an operating system and a host memory storing data. The system further comprises a detector framing node being programmable to receive image data from a selected flat panel detector of a plurality of different flat panel detectors, and communicating the received image data to the host memory independent of the operating system. Claim 28 specifically recites a detector framing node comprising a computer communication interface to communicate image data with a host memory of a host computer over a computer communication bus independently from control of a host processor of the host computer. The detector node further comprises a control unit to receive a plurality of event instructions from the host computer through the computer communication interface, the event instructions selectively controlling events in the detector framing node, a radiation generation system or an image detection system and the control unit executing the event instructions in real time at predetermined timing intervals.

Application number 09/774,552 does not recite the same invention as Applicants' claimed invention. Claims 1-47 of Application Number 09/774,552 are directed to a detector framing node for receiving image data and communicating a portion of the image data to a host computer. The detector node comprises an image detection interface to receive image data in the form of at least one image frame having a predetermined sequence of event instructions constructed off-line, a control unit to select a predetermined portion of the image data received on execution of the predetermined sequence, for storage and a memory unit to store the predetermined portion in response to the selection by said control unit. Applicants' invention is not directed to receive image data in the form of at least one image frame having a predetermined sequence of event instructions constructed off-line. Instead Applicants' invention is directed to a detector framing node programmable to receive image data from a selected flat panel detector of a plurality of different flat panel detectors and communicate the received image data to the host memory independent of the operating system.

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Accordingly, Applicant respectfully submits that the independent claims 1, 28 and 44 are patentably distinct from Applicant's co-pending application No. 09/774,552. Claims 2-27 depend directly or indirectly from claim 1, claims 29-43 depend directly or indirectly from claim 28 and claim 45 depends from claim 44. Withdrawal of the rejections is respectfully requested and allowance of claims 1-45 is respectfully solicited.

Claims allowable over the applied art

The rejection of claims 1-21, 25, 28, 32-37 and 40-45 under 35 U.S.C. 102 (e) on Polichar et al (US patent 6,205, 199) is respectfully traversed. The present invention, as claimed in Claims 1 and 28 and 44 is patentable over the Polichar reference reference. "Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." W.L. Gore & Associates v. Garlock, Inc., 220 USPQ 303, 313 (Fed. Cir. 1983).

Polichar does not teach, suggest or disclose at least the claim recitations as described in the independent 1, 28 and 44 of the present invention. Claims 1 and 44 discloses an image data acquisition system comprising a host computer having at least one host processor executing operations with an operating system and a host memory storing data. The system further comprises a detector framing node being programmable to receive image data from a selected flat panel detector of a plurality of different flat panel detectors, and communicating the received image data to the host memory independent of the operating system. Claim 28 specifically recites a detector framing node comprising a computer communication interface to communicate image data with a host memory of a host computer over a computer communication bus independently from control of a host processor of the host computer. The detector node further comprises a control unit to receive a plurality of event instructions from the host computer through said computer communication interface, the event instructions selectively controlling events in the detector framing node, a radiation generation system or an image detection system and said control unit executing the event instructions in real time at predetermined timing intervals.

Polichar does not teach, suggest or disclose Applicants claimed invention. Specifically, Polichar does not describe an image acquisition system comprising a detector framing node being programmable to receive image data from selected flat panel detectors. Applicants have carefully reviewed column 12, lines 32-49. Nowhere does Polichar teach suggest or disclose a detector framing node being programmable to receive image data from selected flat panel detectors. Polichar merely describes an imaging system comprising an imager operating in a progressive scan mode providing a discrete pixel readout cycle. The pixel clock generator provides a variable frequency pixel clock for operation of the imager in a mode in which the sampling and digitization of each individual pixel is phase correlated. A sample and hold circuit is provided for sampling the discrete pixel readout responsive to the pixel clock and an analog to digital converter is provided for digitizing each pixel as the discrete pixel readout is sampled. An image processor is provided for generating an image from the digitized pixels and a

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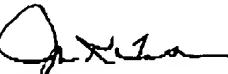
serial communications link between the buffer memory and the image processor. A serial interface driver for transmitting the digitized pixels to the image processor via the serial communications link. (Column 3, lines 27-50). Nowhere does Polichar teach, suggest or disclose an image data acquisition system comprising a host computer and a detector framing node being programmable to receive image data from a selected flat panel detector of a plurality of different flat panel detectors, and communicating the received image data to a host memory independent of the operating system.

Accordingly, Applicant respectfully submits that the independent claims 1, 28 and 44 are allowable over the applied reference. Claims 2-27 depend directly or indirectly from claim 1, claims 29-43 depend directly or indirectly from claim 28 and claim 45 depends from claim 44. Withdrawal of the rejections is respectfully requested and allowance of claims 1-45 is respectfully solicited.

In view of the foregoing, Applicant respectfully submits that the application is in condition for allowance. Favorable reconsideration and prompt allowance of the application are respectfully requested.

Should the Examiner believe that anything further is needed to place the application in even better condition for allowance, the Examiner is requested to contact applicant's undersigned representative at the telephone number below.

Respectfully submitted,

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